PROCESSING, FABRICATION, AND DEMONSTRATION OF HTS INTEGRATED MICROWAVE CIRCUITS

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Short Title of Work: Processing, Fabrication, and Demonstration of HTS Integrated

Microwave Circuits

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DESCRIPTION OF PROGRESS

TASK 1.0: COMPARATIVE TECHNOLOGY ASSESSMENT

This task is essentially complete, but we are continuing to monitor progress in other technologies as they relate to the goals of this program.

TASK 2.1: INTEGRATED SUBSYSTEM SPECIFICATIONS

An analysis has been carried out to determine the effect of HTS preselector filters on the sensitivity and spur-free dynamic range of a microwave receiver. The study is based on the measurements presented in our quarterly report #8 on intermodulation distortion and noise figure in HTS filters. A result of the analysis is that the low noise figure of HTS filters will allow the benefits of preselection without significantly contributing to the system noise figure. In addition, the intermodulation distortion measured so far in HTS filters was found to be low enough not to affect the system spur-free dynamic range, which is generally set by the other nonlinear components in the system.

A paper on this analysis, included here as an Appendix, has been accepted for publication in the 1994 IEEE International Microwave Symposium Digest.

TASK 2.2: FUNCTIONAL COMPONENT AND SUBSYSTEM DESIGN, FABRICATION AND TESTING

Filterbanks

Results on fabricated single channels for the parallel HTSSE-II program were obtained during this reporting period. The design, layout and mask fabrication for the filters were supported by NRL as part of the HTSSE-II program, while the packaging concept and the development of the process and test patterns were part of this ARPA/ONR

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program. It is therefore pertinent that we report here on the fabrication, packaging and experimental results obtained, since the technology will be directly applicable to the EW Cos^3 filters designed for this program (see last report).

- Fabrication

During this reporting period three processing runs (Runs Filter-1, Filter-2, and Filter-3) were completed. A total of eight $LaAlO_3$ substrates, 2-inches in diameter and 20 mils thick, were started and eight filters were produced. Seven of these eight filters had bandpass characteristics that were acceptable for incorporation into the four-channel filterbank. The single exception had excessive insertion loss, possibly due to scratches or defective YBCO in the hybrid coupler. A fourth processing run (Run Filter-4) with four substrates is in progress. The wafer layout for filter channel 1 and associated test circuits is shown in Figure 1. Note that the transition chips for connecting adjacent filter channels in the filterbank are fabricated on the same wafer as the filter.

The process sequence for filters is given in Table 1. It is nearly the same as the sequence given in the last report, except for a few refinements. Annealing of the Au contacts to YBCO is done in a quartz tube furnace by ramping from room temperature to 580°C (rather than 550°C) in 30 minutes, soaking at 580°C for 30 minutes, then cooling to room temperature over a 12 hour period by turning the furnace off. During the entire heating and cooling time, oxygen is flowing through the furnace at a rate of 1000 sccm. The Au plating time has been reduced from 30 minutes to 15 minutes in order to limit the amount of time the substrates are immersed in the plating solution. This solution can sometimes break through the protective photoresist layer and attack the YBCO film. The resulting 2m thickness of plated Au is adequate for a ground plane. The thickness of the resistive Mo layer in the Mo/Ti 50Ω thin film load has been increased from 76 nm (Runs Filter-1 and Filter-3) to 114 nm (Runs Filter-2 and Filter-4) because the sheet resistance at 77K was above the desired 1.0 Ω/□ value. The higher-than-expected value of sheet
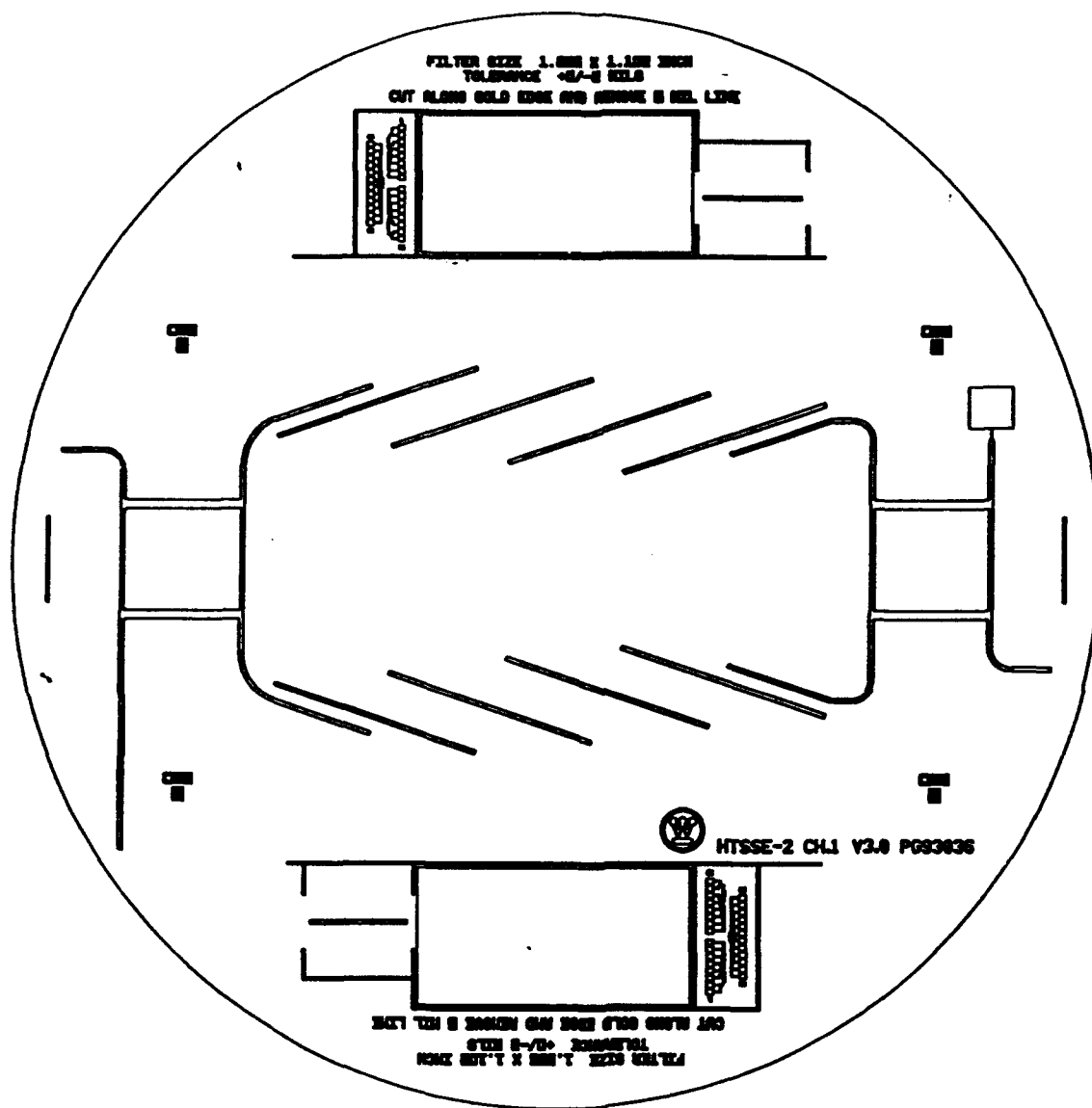
Figure 1. Diagram of layout of channel 1 filter (center), transition chips to facilitate connection of filter channels within a common package (lower left and upper right chips), test pieces for measurement of surface resistance after processing (two blank rectangular chips at top and bottom), and test patterns for measuring dc properties of YBCO and the thin-film Mo/Ti resistors (lower right and upper left chips) on a two-inch wafer.

Table 1. Process Sequence for HTS Filters

Mask	Description	Material	Thickness	Process
1	Contact to YBCO	Au	200 nm	Lift-off
	Contact anneal	Au on YBCO	n/a	580°C ramp in O_2
none	Ground plane base	Ti/Au	20/200 nm	Sputter
	Ground plane thick metal	Au	2 μm	Plate
2	Filter	YBCO	400 nm	Ion Mill
3	Resistor	Mo/Ti	114/10 nm	Lift-off
4	Capacitor and contact pads	Ti/Au	20/200 nm	Lift-off

Note:

- Substrate is 2-inch diameter $LaAlO_3$, 20 mils thick.
- Sputtered epitaxial YBCO film, nominally 400 nm thick, coats one side of substrate.
- Minimum feature size in filter: 10 μm (resistor width).
- Test patterns ($R_{surface}$, R_{sheet}, $R_{contact}$, T_c, J_c) are included on mask set.

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resistance may be associated with Mo leaching oxygen from the $LaAlO_3$ substrate, thereby partially oxidizing the Mo film and increasing its resistance. Mo/Ti films deposited on oxidized silicon test wafers gave the expected sheet resistance, while Mo/Ti films deposited on $LaAlO_3$ substrates in the same run had sheet resistances that were $\approx$50% higher than expected. The possibility that repeated cleanups of the wafer in an oxygen plasma during processing (40 sccm O_2, 50 mT, 135W) may increase the sheet resistance of Mo/Ti resistors by oxidizing the Ti cap and the Mo resistive layer was investigated. Immersing a Mo/Ti test wafer in an oxygen plasma for a total of 20 minutes had essentially no effect on sheet resistance (<1%). however, so the oxygen plasma was judged to be not responsible for the increased sheet resistance. Presumably, the Ti capping layer effectively protects the underlying Mo from oxidation, as intended.

It must be noted here that the value of the resistance obtained is not critical and can be allowed to vary substantially from 50Ω. The reason is that it is used as a termination for the out-of-phase port of the output 3 dB branch-line hybrid (see Figure 1) in each channel. Modelling supports this assertion; in the ideal case of a perfect design, this termination could even be a short circuit without affecting the channel performance.

Better control of ion milling times for patterning the YBCO film has been obtained through the use of a recently-installed end point detector on the ion miller. The detector, a secondary ion mass spectrometer (SIMS), reliably senses Ba+ (138 atomic mass units) while YBCO is being removed and LaO+ (155 atomic mass units) while the $LaAlO_3$ substrate is being removed.

In Run Filter-2 it was found that allowing photoresist (AZ 1350J) to remain in contact with YBCO for an extended time (seven days in this case) results in a residue on the YBCO surface. This residue is soft, in that it can easily be scraped through with tweezers, but it could not be removed by an oxygen plasma, by solvent (acetone), or by mild abrasion. The surface of the residue was examined with a scanning electron microscope at 20,000X and its composition was analyzed by the associated energy

dispersive X-ray spectroscopy (EDS) from 0 to 10 keV. The residue had the form of blemishes, 1 to 2 μm in size, which covered approximately one fourth of the surface area. The EDS spectrum showed a slightly higher carbon peak for the area covered by blemishes relative to adjacent areas, consistent with carbon from the photoresist. The residue was discovered after the plating step, but since no unexpected atomic species were revealed by the EDS analysis, the four wafers in Run Filter-2 were processed to completion. These wafers produced filters having good characteristics, suggesting that the residue does not seriously degrade YBCO surface resistance. Furthermore, prior to any deposition the substrate is cleaned by ion milling or sputter etching. This cleaning may remove the residue so that it does not inhibit adhesion or electrical contact. In spite of the apparently innocuous nature of the residue, a policy has been established to minimize the time during which photoresist is in contact with YBCO in order to avoid the formation of residue.

An improved approach for defining features by lift-off has been demonstrated in Run Filter-4. Previously, all material layers patterned this way (Au contacts, Mo/Ti resistors, and Ti/Au pads) were done using AZ 1350J, a positive photoresist. In Run Filter-4, the Au contacts were defined using AZ 5214-E, an image-reversal (negative) resist. An image-reversal resist facilitates lift-off by having retrograde (backward sloping) sidewalls. This means that photoresist islands do not get sealed up by the sputter-deposited films and so can be dissolved away in the lift-off process easier than can islands of photoresist having positively sloping sidewalls. The two types of resist (positive and image reversal) require masks of opposite polarity (dark field and clear field, respectively), and in the current mask set only the Au contact mask was made in both polarities. Future masks will have a clear field, compatible with the image reversal lift-off process.

- Post-Processing Testing

As can be seen in Figure 1, test patterns are present on the wafer along with the filter pattern for post-processing evaluation. Results from these test patterns are summarized in Table 2 for the four wafers measured to date. Note that the critical temperature of the YBCO film correlates well with room temperature sheet resistance (associated with oxygen content in the chains) and with critical current density, as expected. The Mo/Ti sheet resistances are somewhat higher than targeted, as discussed above.

The large difference in contact resistance (two orders of magnitude) between the wafers from Run Filter-1 and those from Run Filter-3 is attributed to the surface treatment prior to depositing the contact Au. In Run Filter-1, the YBCO surface was ion milled (300V, 80 mA, 1.5 mT Ar, 10 minutes, with rotation) while in Run Filter-1, the YBCO surface was sputter etched (500W RF, 5 mT Ar, 3 minutes, no rotation). It appears that ion milling is superior in conditioning the surface for contact resistance, but in either case the contact resistance is sufficiently low as to contribute negligible filter insertion loss. The YBCO beneath annealed Au contacts or beneath Cr/Au (unannealed) contacts was found to be unaffected by the presence of the contact metals. Essentially zero voltage drop was measured at 77K for current passing through YBCO beneath regions that had received the contact metals. This further supports the contention that contacts do not contribute significantly to filter losses.

Finally, the surface resistance was measured at 77K using the two rectangular pieces shown in Figure 1 in a parallel plate resonator. Values normalized to 10 GHz ranged from 0.71 mΩ to 2.9 mΩ. Surface resistance measurements for the four wafers fabricated in Run Filter-2 gave values of 1.3 mΩ to 1.4 mΩ. Figure 2 shows a calculation of the filter insertion loss at mid-band for a four-pole Chebychev filter with a 50 MHz ripple bandwidth and 0.1 dB of ripple amplitude. A gold ground plane was assumed. The losses were plotted as a function of the surface resistance of the top side, the patterned YBCO

Table 2. Test Results Following Filter Fabrication

Fabrication	Filter-1 W93-019 1	Filter-1 W93-022 2	Filter-3 W93-502 3	Filter-3 W93-503 4
Run				
Wafer				
Filter Channel				
YBCO Film (nominally 0.4 µm thick)				
Sheet resistance at room temperature ($\Omega/\square$)	7.5	8.1	15.7	8.5
Critical temperature after four-mask level process (K)	87.0	90.3	82.0	86.4
Critical current density at 77 K (MA/cm²)	1.0	2.2	0.27	1.2
Mo/Ti Resistor (target value $1\Omega/\square$)[1]				
Sheet resistance at room temperature ($\Omega/\square$)	2.31	2.69	2.51	3.02
Sheet resistance at 77 K ($\Omega/\square$)	1.40	1.85	1.60	2.12
Ratio (RT/LN) of sheet resistance	1.65	1.45	1.57	1.42
Contact Resistance of Au annealed into YBCO[2,3]				
Contact resistance at 77 K (µΩ-cm²)	1.0	0.15	70.	120.
RF Properties[4]				
Surface resistance at 10 GHz and 77 K (mΩ)	0.71	1.4	2.9	N/A

Notes:
1. Resistor value not critical to channel performance.
2. Au annealing conditions: ramp to 580°C in 30 min, then soak for 30 min in flowing O$_2$; cool to room temperature in 12 hours.
3. Magnitude of contact resistance associated with substrate clean prior to Au sputtering; W93-019 and W93-022 were ion milled while W93-502 and W93-503 were cleaned by back sputtering.
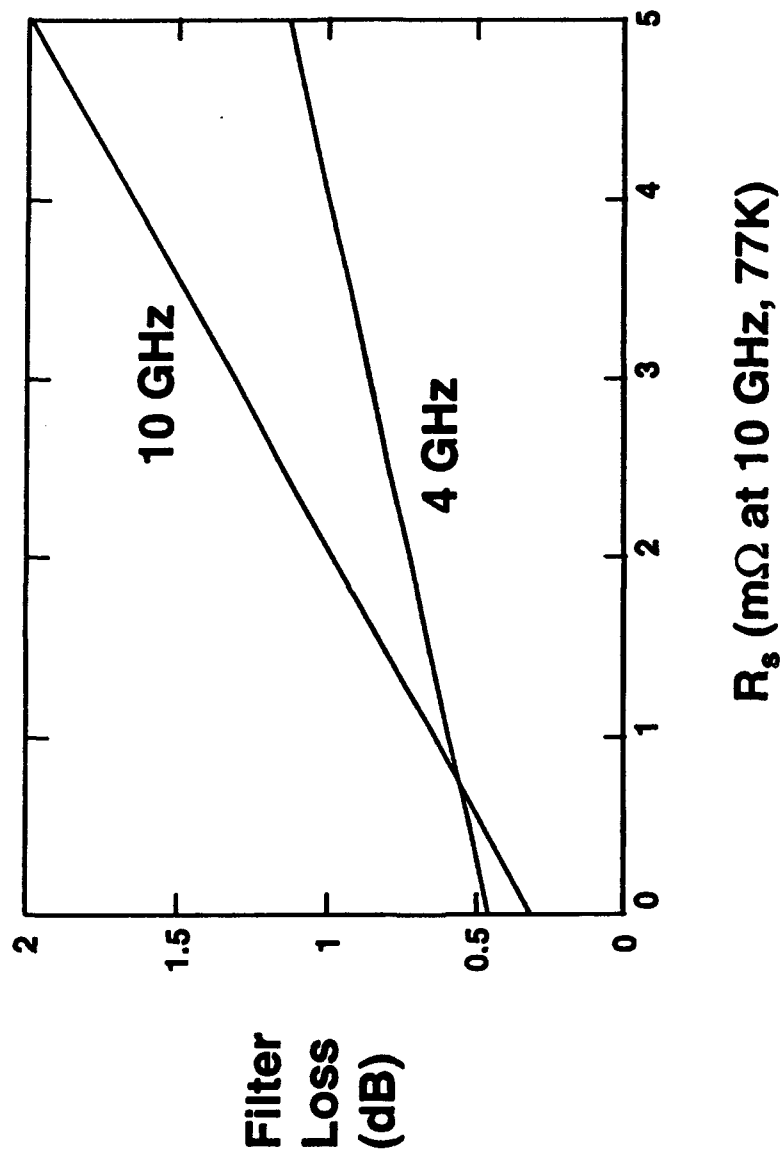4. Surface resistance measured with parallel plate resonator.

Figure 2.   Calculation of filter insertion loss at mid-band as a function of the YBCO surface resistance assuming a YBCO microstrip pattern and a gold ground plane.   Calculation is for a four-pole Chebychev filter with 0.1 dB amplitude ripple and 50 MHz ripple bandwidth, for two center frequencies, 10 and 4 GHz, respectively.

film, for center frequencies of 10 and 4 GHz, respectively. At 4 GHz, the case of the filters in this work, the insertion loss increases by only 0.5 dB from the lossless conductor case to 1 dB at $R_s = 4$ mΩ. Note that the rate of increase is more severe at 10 GHz. Thus, films with post-processing surface resistances of 3 mΩ are quite acceptable for this work.

- Packaging

Since the last report, assembly and testing of channelizer components was accomplished. Packages for testing single filters, for testing two filters with a connecting transition chip, and for the four-filter channelizer itself have been assembled and used, with ultimate complete success. Single channels are soldered to their individual carriers, and are then inserted into the single-filter package for initial testing. After verification of performance, the carrier/filter channel assembly is removed and can be placed into its proper position in the channelizer. This testing and package interchange involves connection of the microstrip lines on the device to pin connectors in the package walls using gold ribbon which is parallel-gap welded to the pin and to the gold pads on the device. No problems have arisen with the bonds on the device due to multiple attachment and/or overlay of new pieces of ribbon. Only one instance of bond failure has occurred, due to a marginal weld of the ribbon to the hemispherical pin end. Subsequently, welding of ribbons to the pins was done with multiple overlapping welds and no further failures have occurred.

The most significant development problems with the packaging have been: 1) the selection of the proper size of the lanthanum aluminate substrate when cutting into rectangular form after device processing, to prevent chipping of the substrate edges during thermal cycling, and 2) solder bond integrity of the substrate to the carrier. The size problem has been ameliorated through increasing the gap between substrate and package wall by cutting the substrates to slightly smaller sizes in length and width. Further work

must be done to improve the accuracy of location of the substrate on the carrier during the soldering process to assure that the gaps are uniform at all four edges of the substrate.

The other problem, that of solder bond integrity of the substrate/carrier assembly, has been solved to the point that degradation of bandpass shape, which had been observed for some filter assemblies, has been eliminated. Soldering of the gold-plated back side (the ground plane side) of the lanthanum aluminate substrate to the gold-plated niobium carrier had been accomplished by inserting an indium solder preform sheet of 0.002" thickness between the two, and supporting the substrate around the edges with a soldering fixture specially made for the purpose. Moderate spring pressure was applied to the carrier and the assembly was heated to about 160°C, a few degrees above the 157°C melting point of indium. Approximately half of the solder (by weight) exuded, and the assembly was cooled. Examination of filter assemblies with deficient bandpass performance established that the indium was failing to wet the carrier surface. This was remedied by pretinning the carrier surface with indium. Further improvement was obtained by increasing the solder temperature to about 200°C and increasing the pressure on the substrate. Tests to determine the effect of higher temperatures on the film properties, when the films were heated in air for times much longer than typically necessary for soldering, established that 200°C was safe. Other tests established that indium was not degrading the HTS films by diffusing through the gold layer and reacting with the YBCO. This is crucial in the case where HTS films on both sides of the substrate must be used, as for the delay lines, to obtain the lowest possible device insertion loss.

- Results on Single Channels

Figure 1 shows the layout of one of the HTSSE-II channels (Channel 1), including the two identical filters, the two identical branch-line hybrids and the 50-Ω thin film termination. These are Chebychev filters. The design procedure was reported on last quarter. Figure 3 shows a sample Channel 1 response for one of the wafers fabricated.
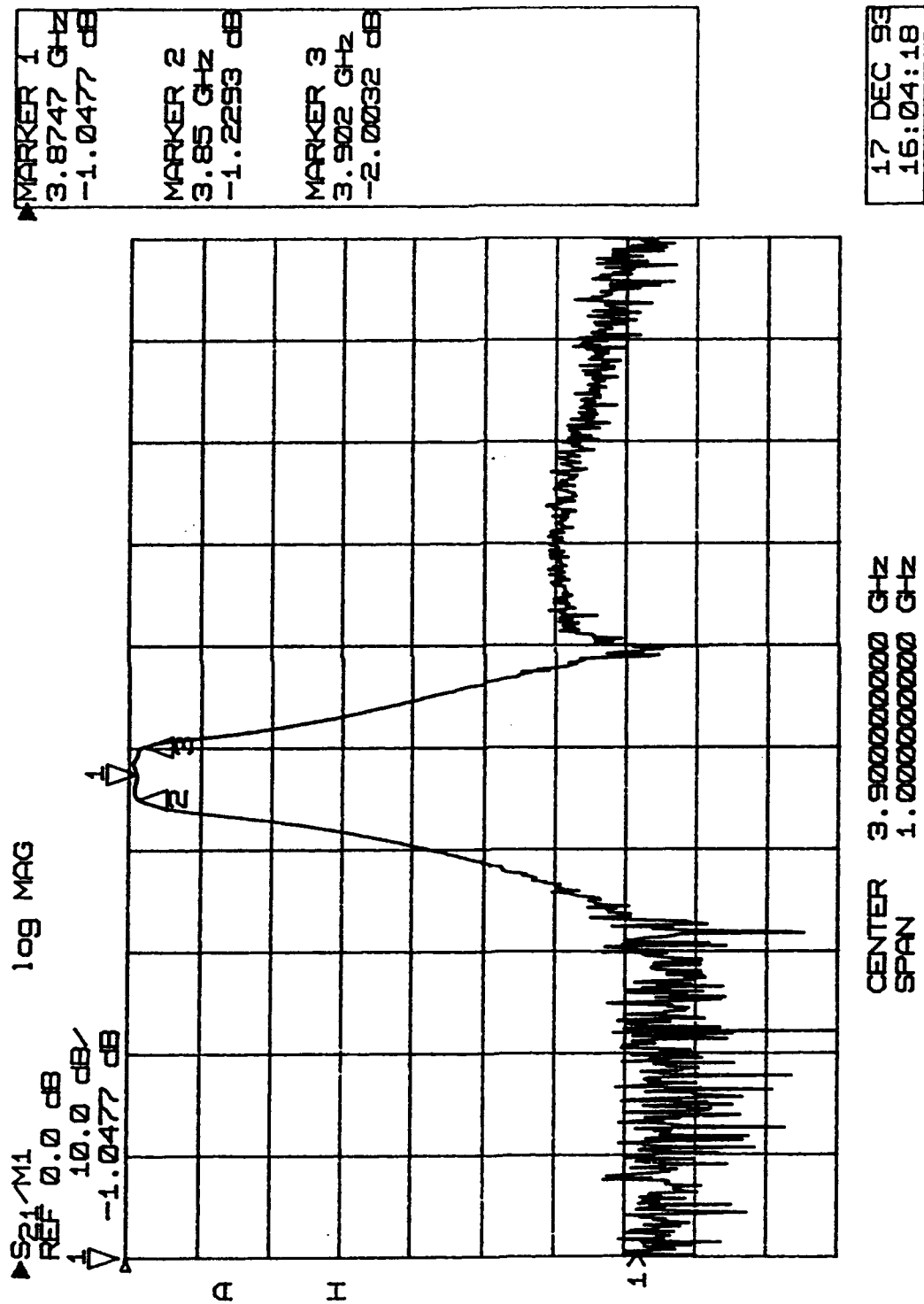
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Figure 3. Transmission response for one of the Channel 1 wafers fabricated, showing low insertion loss, excellent passband shape and a 50 MHz bandwidth, as designed.

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The ripple bandwidth is 50 MHz, as designed. The response shown in Figure 3 has excellent characteristics and shows that the design and fabrication procedures are well in hand.

- Filterbank

Figure 4 is a photograph of the HTSSE-II multiplexer with the top lid removed. The interconnection between channels was made using small sections of microstrip line connected to the channels with short, gap-welded gold ribbons. Figure 5 shows this interconnection in greater detail. The quality of these channel interconnections is critical to the success of this approach. At this time the optimization of these transition chips is underway in order to attain minimum insertion loss and channel distortion. This is being accomplished by using a double-channel package which, by requiring the use of only one channel interconnection, makes the optimization easier. Results on the four channel multiplexer will be reported in the next quarter.

Delay Lines

Each 22 ns stripline YBCO delay line requires a pair of two-inch wafers. The wafers are 10 mil thick LaAlO$_3$ with a 0.4 μm thick epitaxial YBCO film on each side. Two wafers are used to obtain a stripline geometry. On the bottom wafer, a continuous 1.5m long spiral is patterned into one YBCO film while the film on the opposite side of the wafer serves as a superconductive ground plane. On the top wafer, a spiral line is patterned which is the mirror image of that on the bottom wafer; the YBCO film on the opposite side is a ground plane. When the device is assembled, both spirals are brought into intimate contact. This is done in order to eliminate the effect of air gaps which will inevitably form between the two 2-inch diameter wafers. Air gaps between substrates when only one spiral is present cause forward coupling between adjacent spiral turns, resulting in degraded performance. Our calculations show that the alignment between the
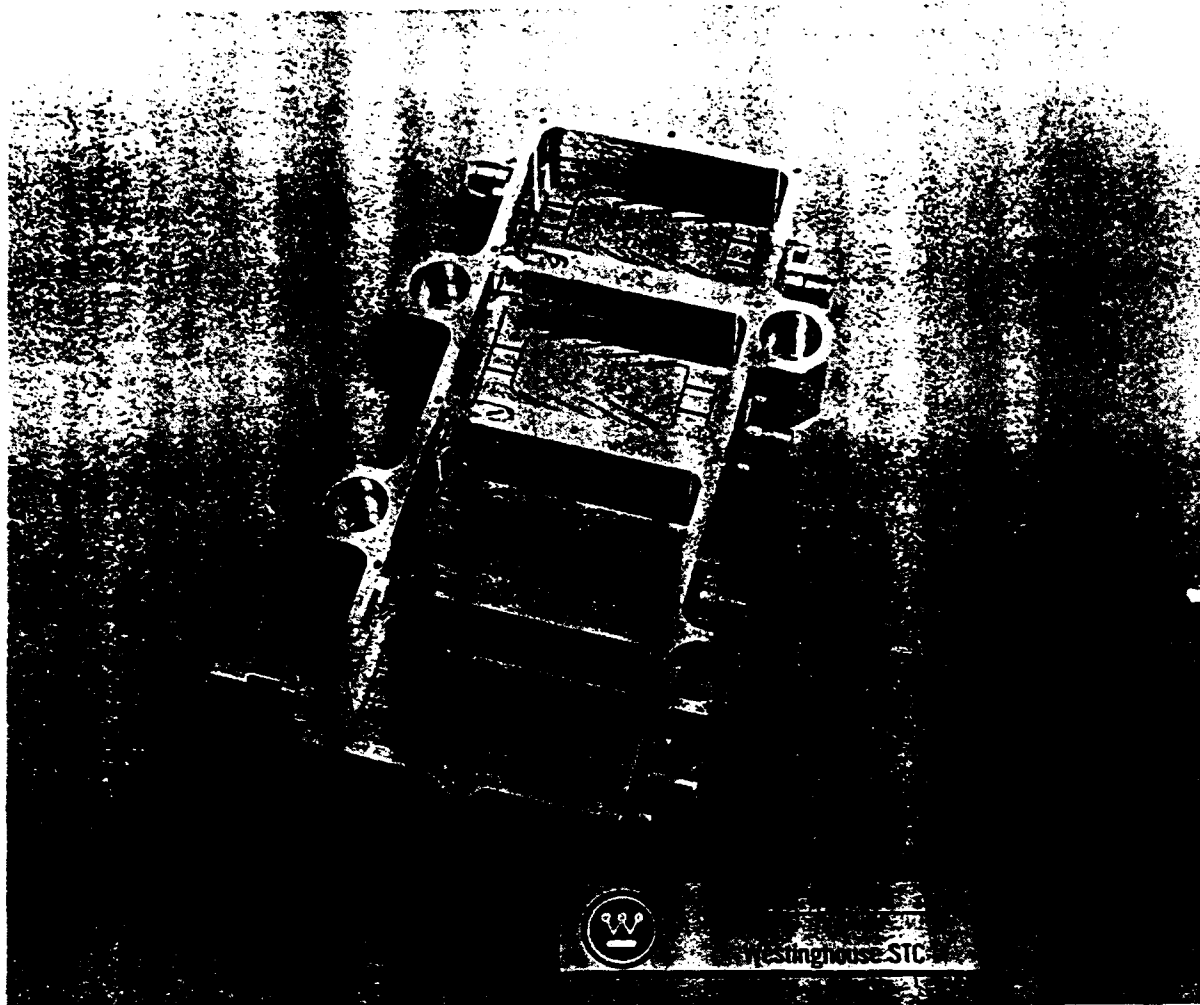
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Figure 4. Photograph of the HTSSE-II multiplexer without the top lid. The connection between channels is accomplished through microstrip transition chips bonded to the channels.

Figure 5.   Close-up photograph of one of the transition chips interconnecting two filterbank adjacent channels.

two spirals must be of the order of 10 to 15 μm when the two wafers are assembled into a packaged delay line. The bottom wafer has coplanar contacts for input and output, as shown in Figure 6. In order to achieve a 50Ω input impedance, the bottom YBCO spiral starts and ends with a width of 22 μm. Within the first turn of the spiral, the width gradually broadens to 150 μm in order to relax the requirements on the YBCO film quality.

- Fabrication

During this reporting period, mask drawings were completed for the pair of wafers which comprise the spiral delay line, and the four masks in the set were fabricated by Micro Mask, Inc. The process sequence for fabricating delay lines using these masks is outlined in Table 3. Note that both top and bottom wafers have spirals and annealed Au contacts to the ground plane YBCO. The purpose of the Au is to facilitate soldering the wafers into the microwave package. The bottom wafer has annealed Au contacts to the spiral while the top wafer does not. However, the top wafer must have holes milled into the Au/YBCO ground plane to enable alignment of the top wafer relative to the bottom wafer. This alignment is accomplished with the aid of alignment marks defined on the wafers for this purpose. Because the delay line occupies nearly the entire two-inch wafer, there is no room for test circuits as there was for the filter wafers. Consequently, a determination of the success of the processing is given by the performance of the delay lines directly.

Three processing runs (Runs Delay Line-1, Delay Line-2, and Delay Line-3), each with two wafers, were initiated and completed during this reporting period, thereby providing six wafers for three delay lines.

- Packaging

The same soldering problems apply to the delay line substrate/carrier assemblies as to those of the channelizer. The same solutions have been found to be effective in
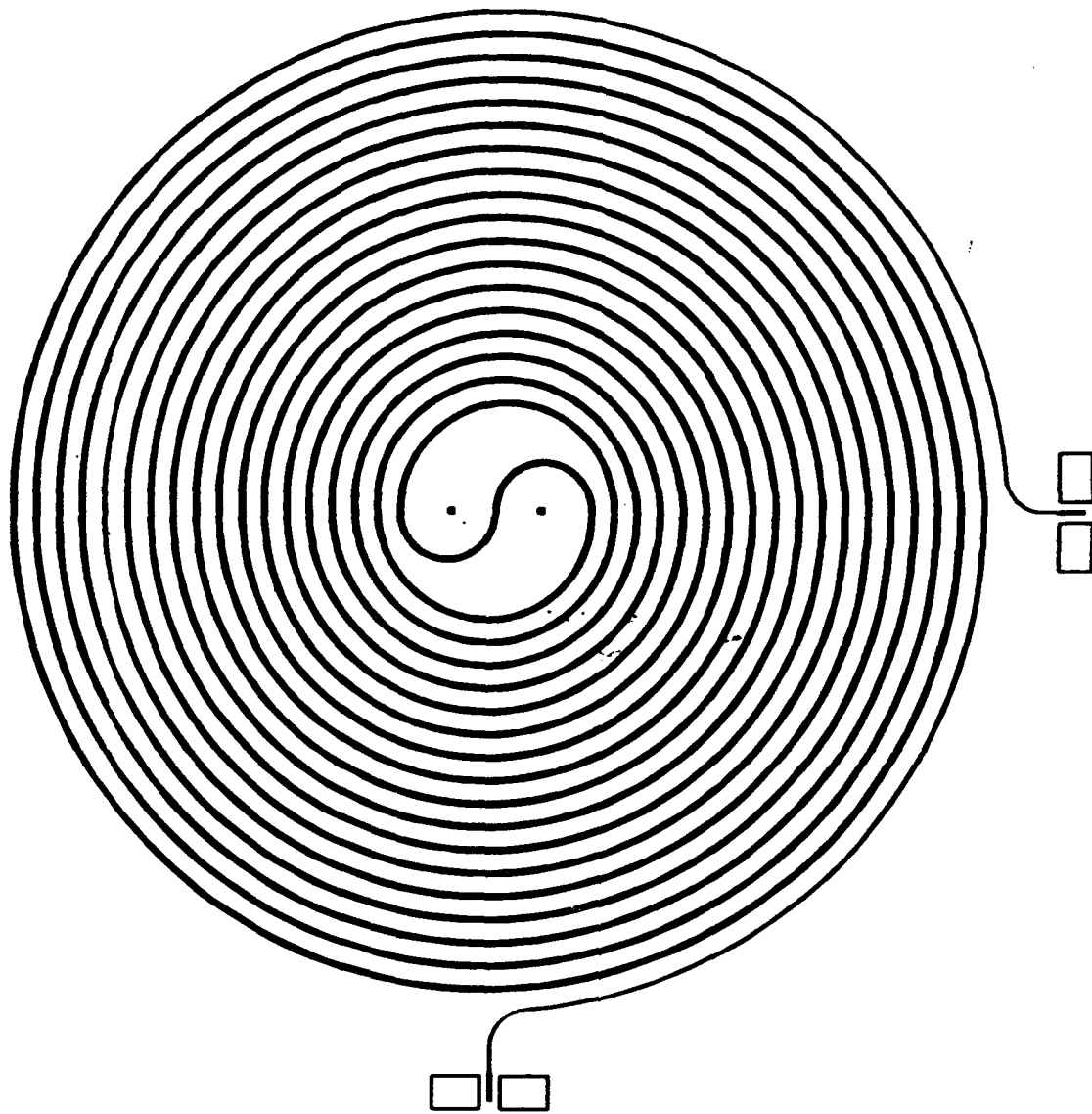
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Figure 6. Diagram of spiral delay line, including coplanar input and output, suitable for a two-inch wafer. This YBCO spiral, with contacts, is patterned on the bottom wafer of the two-wafer delay line assembly; an image YBCO spiral, without contacts, is patterned on the top wafer of the assembly.

TABLE 3. Process Sequence for HTS Delay Lines

Mask	Description	Material	Thickness	Process
Bottom Wafer				
none	Ground plane contact	Au	200 nm	Sputter
	Contact anneal	Au on YBCO	n/a	580°C ramp in O_2
1B	Contact to YBCO spiral	Au	200 nm	Lift-off
	Contact anneal	Au on YBCO	n/a	580°C ramp in O_2
2B	Delay line spiral	YBCO	400 nm	Ion Mill
Top Wafer				
none	Ground plane contact	Au	200 nm	Sputter
	Contact anneal	Au on YBCO	n/a	580°C ramp in O_2
2T	Delay line spiral (image)	YBCO	400 nm	Ion Mill
3T/B	Ground plane holes	Au/YBCO	200/400 nm	Ion Mill

Notes:
- Substrate is 2-inch diameter $LaAlO_3$, 10 mils thick.
- A sputtered epitaxial YBCO film, nominally 400 nm thick, coats each side.
- YBCO spiral has a width of 22 µm at the beginning and end, tapering to 150 µm over most of the length.

improving the microwave characteristics of the devices. The other critical packaging issue for the delay line is that of establishing and maintaining alignment between the delay line spirals on top and bottom substrates. The alignment method has so far worked very well. Alignment of top and bottom is performed using the alignment marks and viewing holes described in the last report. The top and bottom carriers are then held in this alignment by pins in clearance holes. A decision was made to use a low melting point fusible bismuth alloy injected between pin and wall of the clearance hole to fix the horizontal alignment. This is reversible, whereas use of epoxy would be permanent. Because this bismuth alloy is well supported by the pin/hole structure, its strength, which is low for this type of alloy, is not critical. Vertical contact pressure is established by use of nuts and Belleville spring washers on the threaded ends of the alignment pins. The compression resistance of the spiral spring which makes ground contact between top and bottom carriers around the periphery of the delay line substrates must be overcome by the tightening of the four alignment pin nuts to bring the substrate surfaces into contact. The point at which this occurs can be easily seen by observing the focus of the alignment marks using a suitable microscope. Indeed, a calibrated focus adjustment on the microscope allows accurate measurement of the interface gap until they are brought into contact. Preload is then placed on the substrates by further slight tightening of the nuts which applies adjustable pressure through the Belleville spring washers. After alignment and preload are established, the nuts and washers are removed one at a time for application of the bismuth alloy between the pin and clearance hole. The nuts and washers are then reinstalled. Only negligible alignment changes have been observed to occur through this removal and reinstallation procedure.

After the alignment of the carrier assembly has been completed, the assembly is installed in the housing, contacts are bonded, and the package is closed with mounting plate and lid. The two delay line assemblies are coupled by mating SMA connectors when brought together on the mounting plate.

-Delay Line Results

Figures 7(a) and 7(b) show the transmission response at 77K in the frequency and time domains, respectively, for the first delay line made using this approach. The delay is 22 nS and the amplitude ripple is about 2 dB over most of the 4 GHz band. The characteristics obtained are excellent already and demonstrate the effectiveness of the technique developed for low loss, low cost, wide band delay lines. These results are a significant improvement over those obtained from the previous approach (see Quarterly Report #7), which had high amplitude ripple due to forward coupling between turns of the spiral line and due to the coaxial line connections. Our measurements on the new delay line show that the forward coupling problem has been eliminated by the mirror-image spiral on the upper substrate of the stripline configuration (see our last Quarterly Report).

The delay line characteristics will be improved in the next reporting period by refining the packaging technique, especially in the connector region, where the the most significant discontinuities causing the remaining amplitude ripple occur.

TASK 3.1: PVD MULTILAYER FILM FABRICATION

The two subtasks scheduled for this reporting period required delivery of YBCO films on both sides of two-inch diameter substrates to Task 2.2, and development of a multilayer deposition capability on four-inch wafers. Sputter-deposition of YBCO films on 2-inch wafers has stayed ahead of device fabrication requirements. As mentioned in previous reports, the only variable in the production process that has prevented a 100% film yield is the homogeneity of YBCO sputtering targets. Several new types of targets made from different starting powders were obtained from each of two target vendors and were evaluated during the quarter. The targets were generally pressed from finer powders and had a higher density. However, none of the high-density targets performed as well as the ~75% dense targets that had been in use. At this time, the only way to have
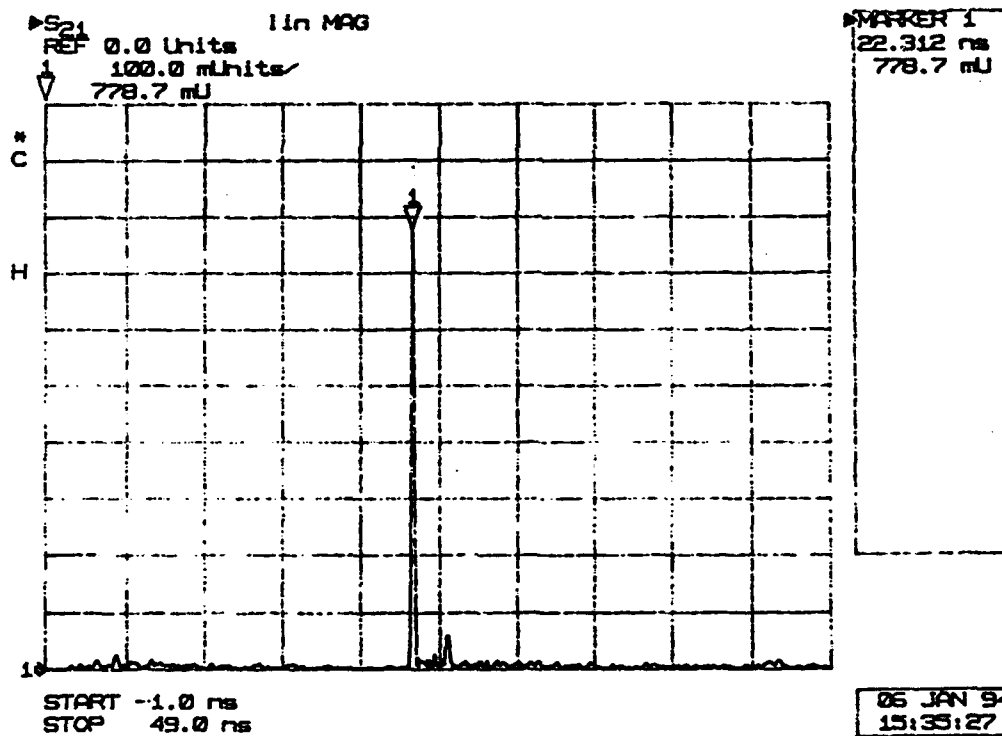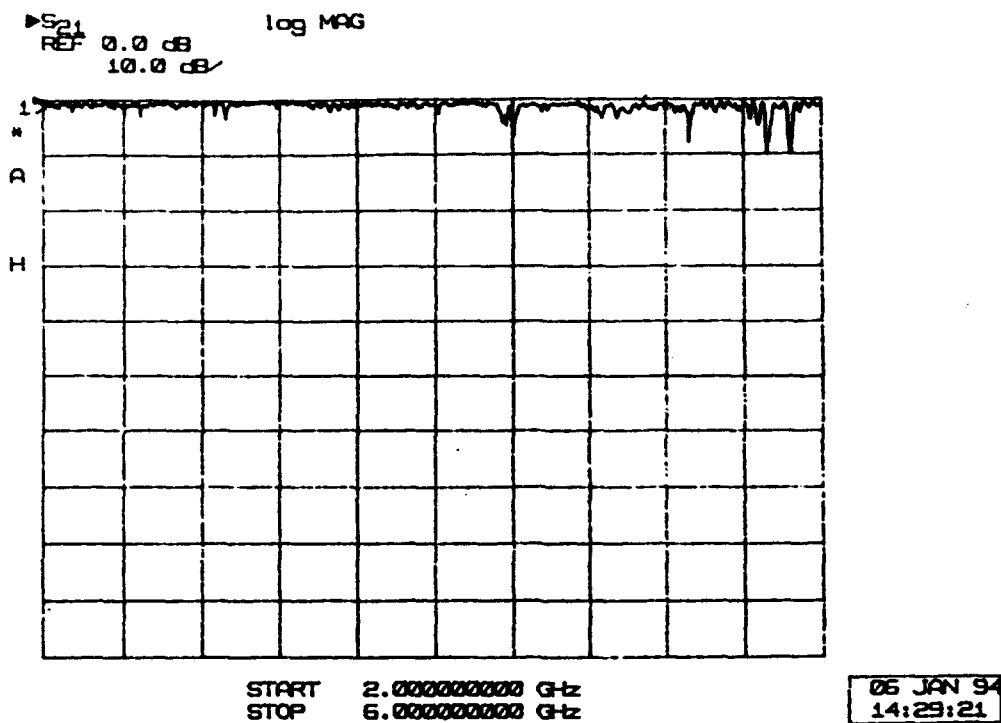
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Figure 7.   (a) Frequency- and (b) time-domain responses for the first delay line made
with the new stripline approach, showing excellent amplitude characteristics
between 2 and 6 GHz (a) and 22 nS of delay (b).

confidence in film properties is to measure rf surface resistance of the first one or two films made from each new target.

One of the deposition parameters that should be readjusted for each target is the partial pressure of oxygen used during the cooldown from deposition temperature. A common misconception is that the highest possible oxygen pressure is best. It has recently been confirmed in a number of laboratories, including Westinghouse, that the optimum oxygen composition of $YBa_2Cu_3O_x$ is $6.90 < x < 6.95$. Higher values of x, in the range of 6.97, can be obtained by cooling in a full atmosphere of oxygen but T_c will be depressed by 4 to 6 Kelvin. Until last quarter, a cooldown pressure of 25 torr O_2 was assumed to be optimum in all cases. It is now clear that the optimum partial pressure may be as low as 5 torr depending on which particular target is used. The current speculation is that this change is related to efforts by target suppliers to reduce the carbon contamination in their product. These considerations are unimportant for filters at 4 GHz since filter properties are fairly independent of R_s once it is reduced to $<1-2$ mΩ. However, for delay lines, any additional improvements in R_s will result in a lower insertion loss.

As in the previous quarter, a very low level of effort was expended in the development of YBCO-coated four-inch wafers using a new sputtering chamber built to a Westinghouse design by Nordiko Ltd., which can accommodate 2, 3, or 4-inch wafers. Although modifications to the thermal design had reduced the heater power needed to maintain the desired substrate temperature from an initial value of 70% to less than 30% of the heater's 2.6 kW maximum, rotary feedthroughs in the vicinity of the heater were overheating during long deposition sequences. Nordiko re-designed these feedthroughs so they are water-cooled, rebuilt them, and delivered them to Westinghouse in August, 1993. The modified feedthroughs were found to be poorly designed, leading to vacuum leaks and loss of the ability to monitor wafer temperature during growth. Nordiko has redesigned and fabricated another feedthrough yet to be delivered.

TASK 3.2: MOCVD MULTILAYER FILM FABRICATION

Work under this task progressed rapidly during the quarter. Emcore delivered the first 2-inch diameter wafers coated with YBCO to Westinghouse for evaluation of rf surface resistance, R_s (77K). The first of these, deposited at 700°C in a partial pressure of 1 torr of oxygen, had a very high value of R_s. A deposition temperature of 700°C is typically used for growth of sputtered YBCO films in oxygen partial pressures of 40-100 mtorr. On the basis of an observation by Hammond and Bormann (Physica C Vol. 162-164, 1989) that the best YBCO films are grown along the decomposition line as shown in Figure 8, we suggested that Emcore increase the growth temperature in subsequent depositions. As a preliminary test, the films deposited at 700°C were annealed in oxygen at 750°C and R_s was remeasured. Chips taken from both the center and edge of a wafer showed improvement in R_s after the anneal. Figure 9 shows the reduction in R_s (77K, 10 GHz) when growth temperature was increased to a maximum temperature of 770°C. The error bars indicate the difference between high and low R_s values obtained for wafers grown at each of three deposition temperatures. The two best wafers, deposited at 770°C, had R_s (77K, 10 GHz) = 1.7 and 2.0 mΩ, respectively. Such values are sufficient for bandpass filters (although other properties such as linearity and power handling have not been measured for MOCVD-grown films), but they are a factor of 3-4 higher than obtained for good sputtered films used thus far in the program for device fabrication. Although the present substrate heater was not designed for higher temperatures, Emcore will try to raise growth temperatures until some minimum R_s is reached.

Sufficient progress was made in lowering the surface resistance of single-sided films to start depositing films on both sides of 2-inch diameter $LaAlO_3$ wafers. A stainless steel substrate holder was fabricated at Emcore and sent to Westinghouse for gold plating. Gold was selected as an appropriate material to be in contact with the surface of the first YBCO film while the second was being deposited based on results
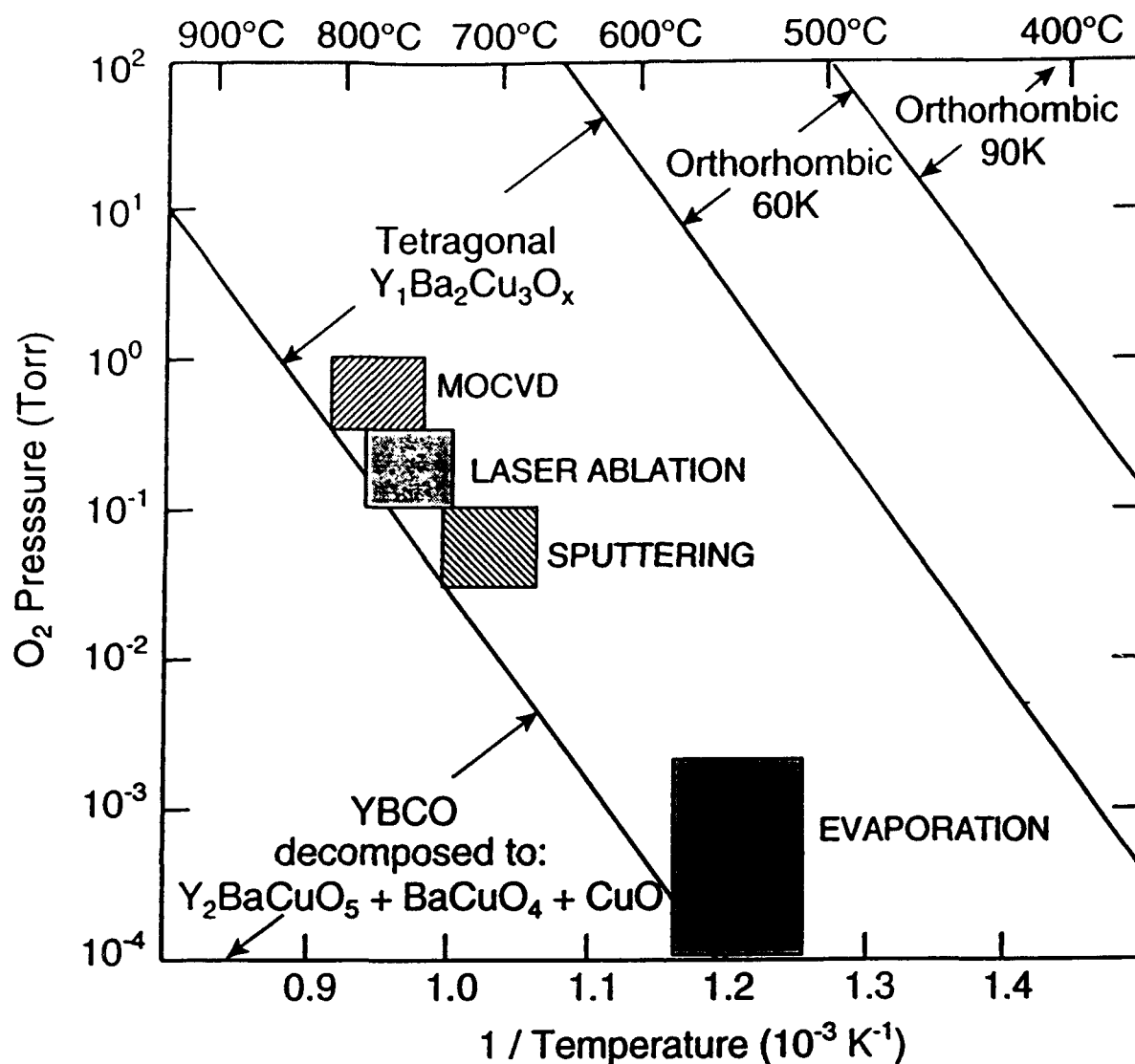
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Figure 8.   Oxygen phase diagram of YBCO. Hammond and Bormann observed that high-quality YBCO films grown by different techniques tend to fall on the line separating the tetragonal phase of $YBa_2Cu_3O_x$ from decomposition into three other phases. Since MOCVD growth can be performed in the highest oxygen partial pressure, this idea suggests that a higher deposition temperature is required than for the other techniques.
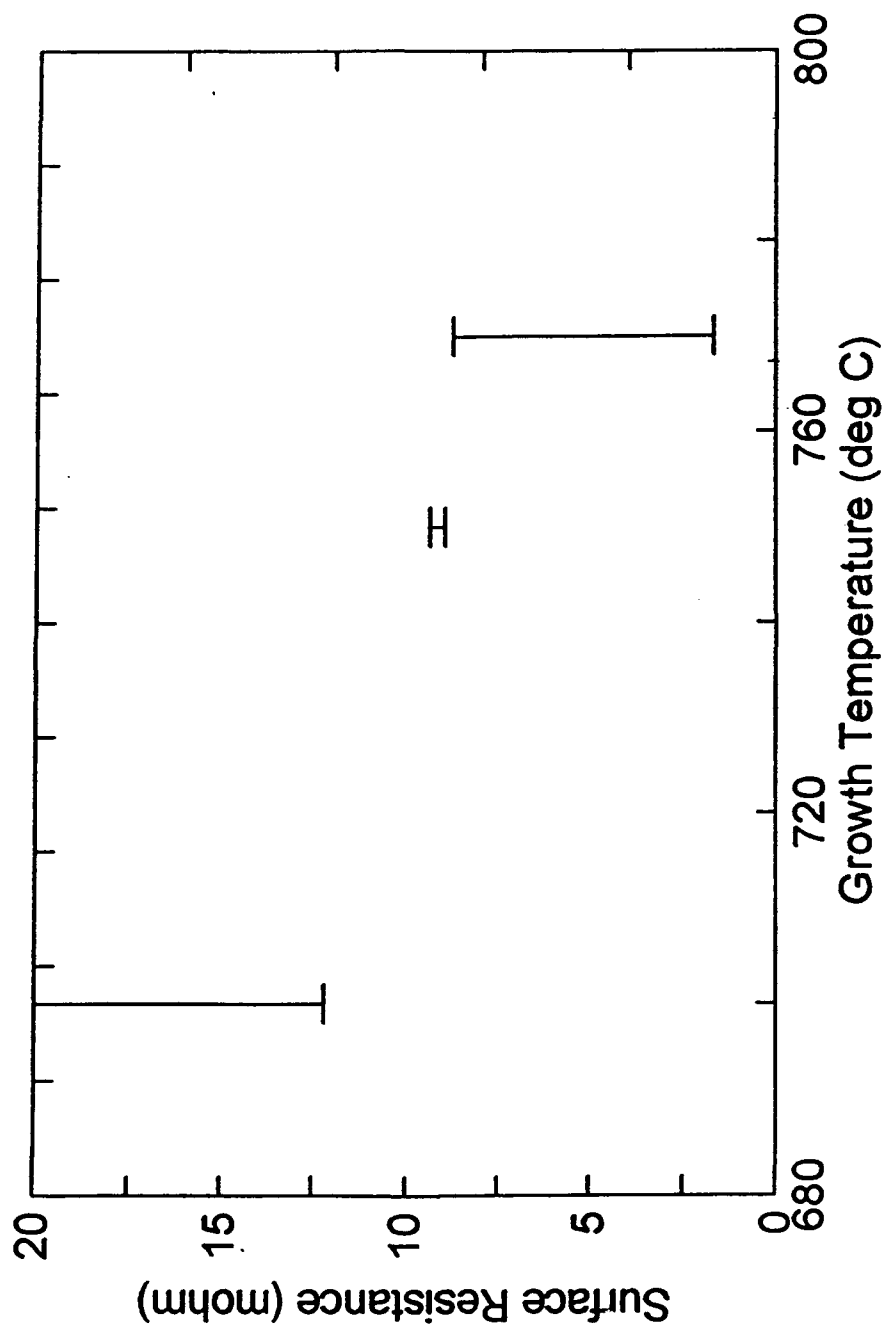
Figure 9. rf surface resistance at 77K and 10 GHz plotted as a function of growth temperature for MOCVD films. The error bars indicate the highest and lowest values obtained for wafers grown at each temperature. The best R_s values, 1.7 and 2.0 mohms, were obtained for two films grown at the highest temperature.

from the Naval Research Laboratory (Desisto et al., Appl. Phys. Lett. Vol. 62, 1682, 1993). (For double-sided films grown by sputtering at Westinghouse, a blank $LaAlO_3$ wafer is placed in contact with the surface of the first YBCO film.) The first batch of double-sided films was deposited and had high transition temperatures and sharp superconducting transitions for films on both sides. These films were not sent to Westinghouse in time for R_s measurements to be made by the end of the quarter. The Ba-thd precursor used at Emcore for all YBCO films grown during the quarter was supplied by Northwestern University. Emcore will not start their evaluation of the new more-volatile precursors, bis(tri-butylcyclo-pentadienyl)barium, (CptBu3)2Ba, and bis(di-butylcyclo-pentadienyl)barium, (CptBu2)2Ba, until the current process is under better control and a backlog of double-sided wafers is produced. A new TGA/DTA instrument was installed at Northwestern University which permitted a more complete evaluation of the vapor pressure and stability of the new compounds to be performed there.

TASK 3.3: RF CHARACTERIZATION OF FILM PROPERTIES

A total of 45 rf surface resistance measurements were made during the quarter on YBCO films on 2-inch wafers. The measurements fell into three categories:

1. Ensure that films sputtered from new targets were qualified for device fabrication.
2. Determine whether any specific device processing steps resulted in degradation of film quality.
3. Evaluate films made by MOCVD at Emcore.

TASK 5.0: SWITCHED FILTERBANK

The design phase of the Etch-Back FET switches is progressing well and will be completed in the next reporting period. Three basic electrical designs for the switch will

be implemented: A nominal design and high isolation and low insertion loss designs. The calculated characteristics (insertion loss and isolation) for each design are shown in Figures 10(a) through (c), respectively. Figure 11 is a layout of one of the switches, showing four Etch-Back FETs, coplanar transition pads and bias lines. The various designs and layouts are at present being integrated into a mask set for 3-inch diameter GaAs wafers.
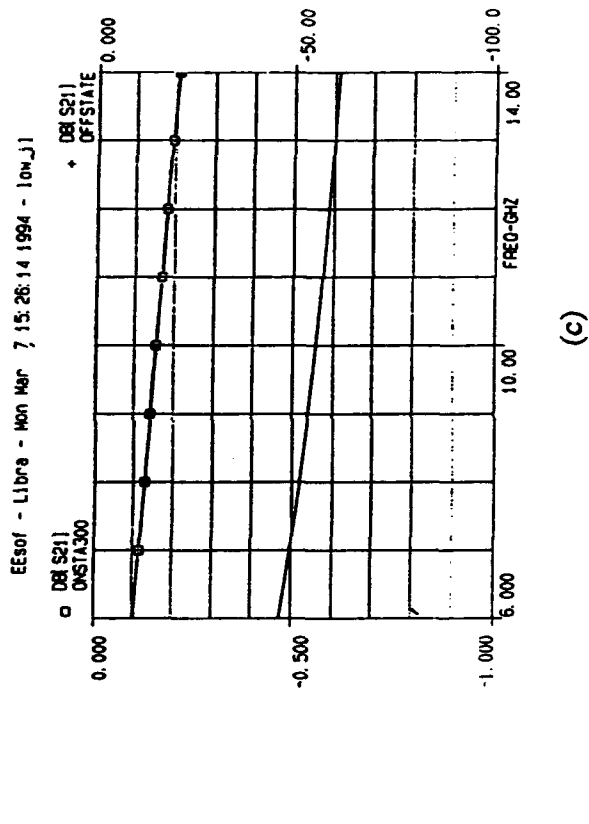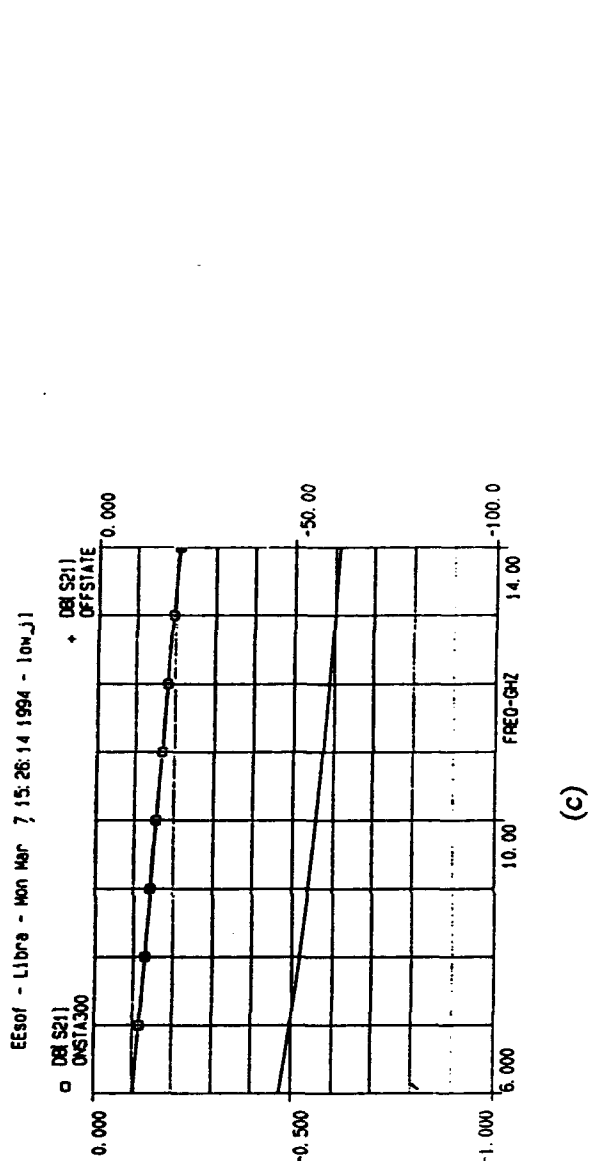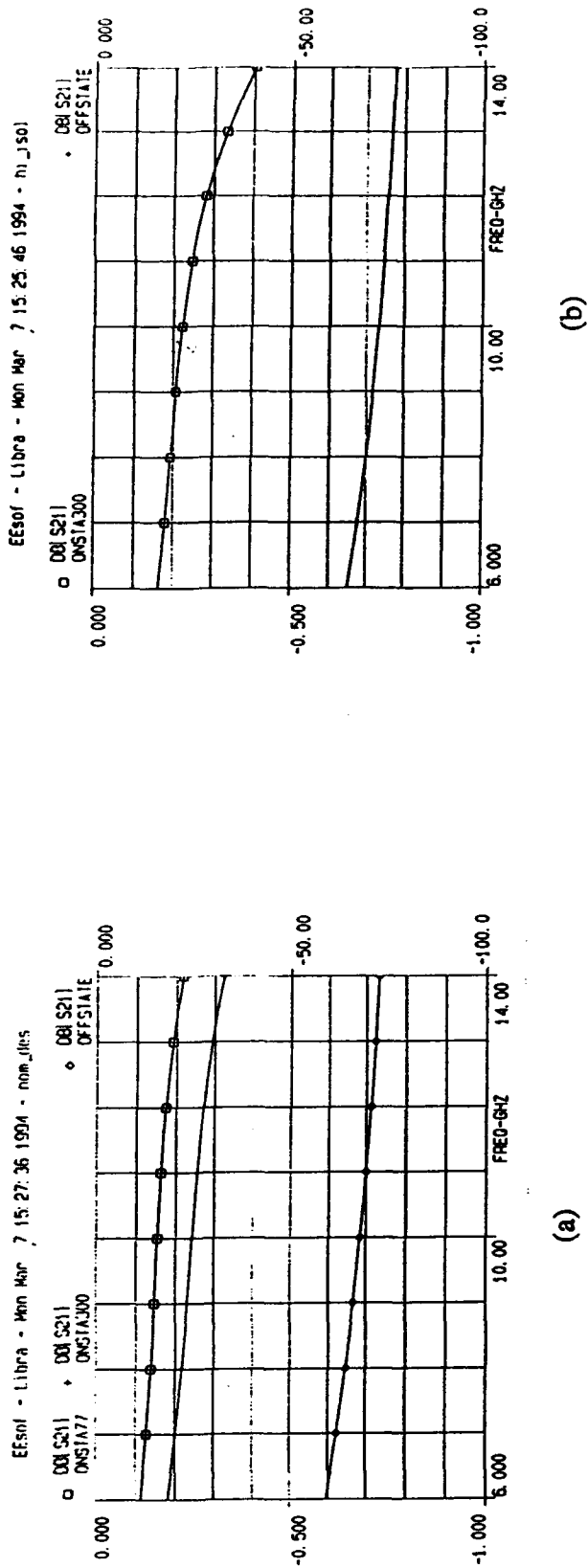
Figure 10. Calculated insertion loss and isolation for the nominal (a) high isolation (b) and low insertion loss (c) designs, respectively.
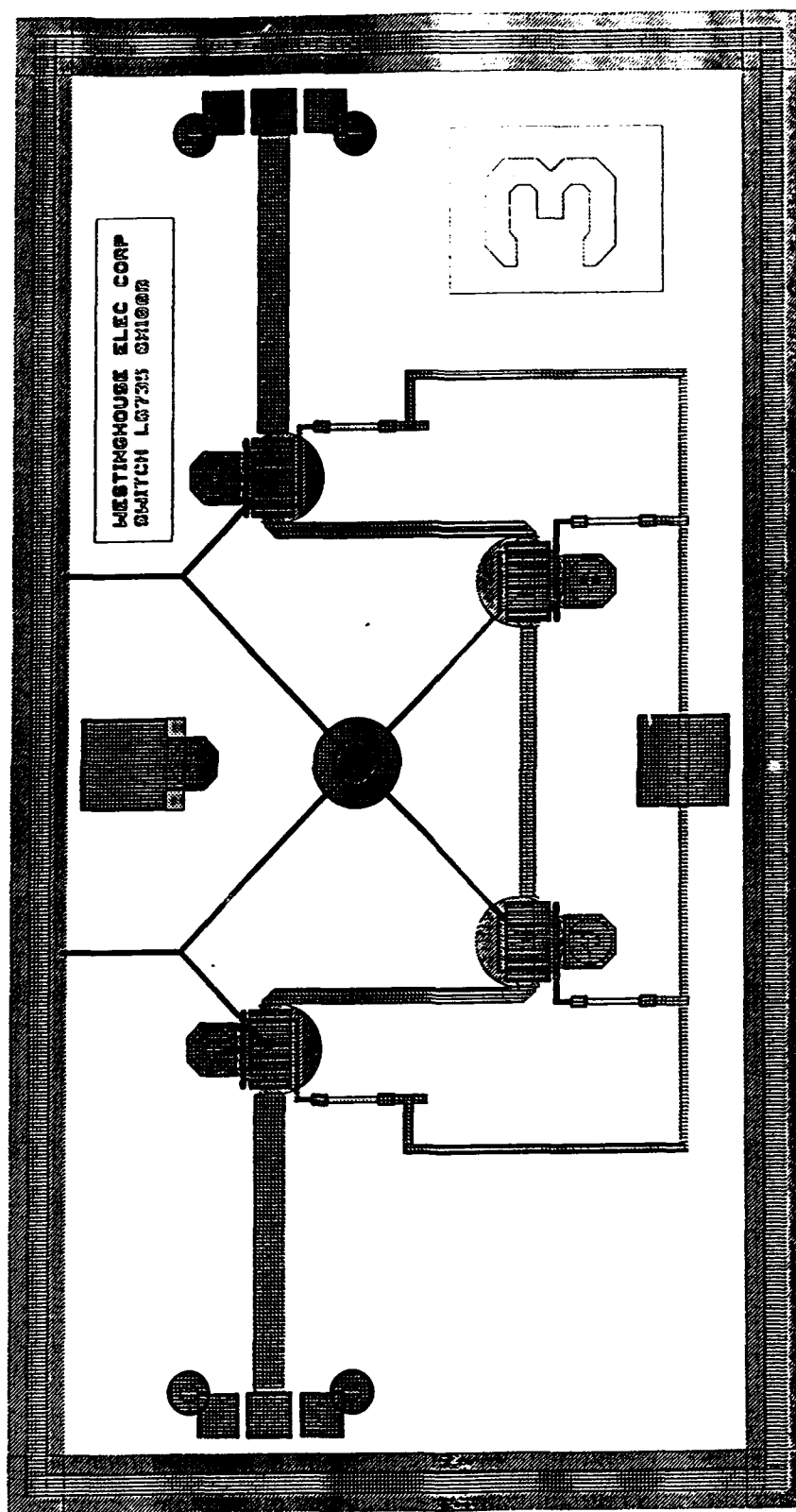
Figure 11.   Representative layout for one of the Etch-Back FET Switches being designed.

PROBLEMS ENCOUNTERED AND/OR ANTICIPATED

Although the start date of this program was July 24, 1991 with the approval of anticipatory spending, the contract was not signed until September 30, 1991 when the first increment of funding was received. The work effort was slowed at DARPA's request to stretch the FY92 funding through 12/31/92. However, FY93 funds were not received until March 30, 1993. These funding limitations have placed the program six months behind schedule.

FISCAL STATUS

Amount currently provided	$5,316,013
Expenditures and commitments through 1/30/94:	3,400,984 *
Funds required to complete:	1,199,223
FY94 funds required:	228,717

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*Includes $512,806 committed to subcontractors and purchase orders.

APPENDIX

DYNAMIC RANGE CONSIDERATIONS FOR
HIGH-TEMPERATURE SUPERCONDUCTING FILTER
APPLICATIONS TO RECEIVER FRONT-ENDS

DYNAMIC RANGE CONSIDERATIONS FOR HIGH-TEMPERATURE SUPERCONDUCTING FILTER APPLICATIONS TO RECEIVER FRONT-ENDS

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Abstract

Planar thin-film high-temperature superconducting (HTS) filters offer very low loss and, when multiplexed into filterbanks, the potential for smaller volume than conventional technology filters of comparable performance. In this paper the issues concerning the application of HTS filters to preselection in microwave receiver front ends will be addressed. These issues include noise figure, third order intermodulation distortion and spur-free dynamic range. The reasons to evaluate HTS filters for these applications are: 1) HTS filters contribute negligible system noise figure because they not only have low loss but operate around 77K and 2) they are nonlinear devices. Our measurements and calculations show that HTS filters in the front end of microwave receivers will allow all the advantages of preselection without contributing significantly to the system noise figure. On the other hand, even though HTS filters are nonlinear, the upper end of the dynamic range will most likely be set by the rest of the receiver chain, not by the HTS preselector.

Introduction

Front end preselection is important in many microwave receiver applications, in order to partition the operational bandwidth into smaller bands. This has the advantage of rejecting unwanted signals that might interfere with the receiver's operation and prevent saturation of the low-noise amplifier (LNA) by those unwanted signals, resulting in degraded performance. Also, front-end filtering can simplify the receiver's architecture by reducing the filtering requirements after mixing, to eliminate unwanted mixing products. However, if the preselector filter has a high insertion loss the receiver noise figure will be adversely affected, resulting in unacceptable system performance for some applications.

High-temperature superconducting (HTS) filters offer the advantage of very low loss in a relatively small volume over a wide range of frequencies. In addition, their noise figure is lower than their insertion loss because they operate at temperatures around 77K. This suggests that HTS filters are suitable for front-end preselection applications.

HTS filters are, however, non-linear devices [1]. Therefore it is important to explore the effect of the filter noise figure and third-order intermodulation distortion on the receiver sensitivity and spur-free dynamic range. The calculations presented of system noise figure and spur-free dynamic range are based on the simplified diagram shown in Figure 1. The HTS filter preselector is assumed to be the first component in the receiver chain, after the antenna. The rest of the receiver is grouped together into a "cascade" of components, the most significant of which is the LNA, usually placed immediately behind the antenna or after the preselector if one is used. The LNA is a significant contributor to the system sensitivity and dynamic range.
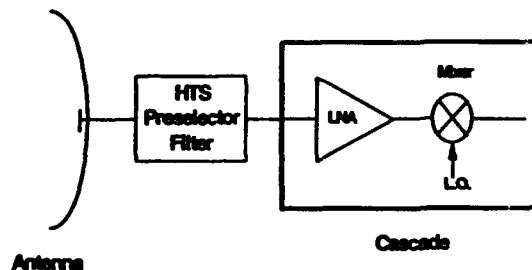

Figure 1 - Simplified block diagram of a receiver front end used to perform the calculations in this paper. The receiver front end is broken up into a preselector filter and a "cascade" of components which groups together the low noise amplifier, mixer, etc.

Noise Figure

The (thermal) noise figure in passive devices is given by the expression [2]

$$F = 1 + (L - 1) \, T / 290,$$

where F is the noise figure, L is the insertion loss and T is the device temperature in Kelvin. Both F and L are expressed as a fraction of 1, not in dB. Notice that at the reference (room) temperature of 290K the noise figure is equal to the insertion loss in the device.

Figure 2 is a calculation of the noise figure of a passive device (e.g. a filter) as a function of insertion loss for two ambient temperatures, 290K and 77K. These curves show that the noise figure is significantly improved by cooling. Although when using conventional materials the loss will also be somewhat reduced by cooling, dramatically lower insertion loss will be achieved by using HTS, resulting in an even lower noise figure.

In terms of a receiver front end, the noise figure was calculated assuming it has the simplified configuration shown in Figure 1. Figure 3 shows the calculated effect of the filter on the system noise figure, as a function of the noise figure of the Cascade of components following it. Three cases are shown, one for a HTS filter with 0.2 dB of loss (NF = 0.054 dB) and two for conventional room-temperature filters with 1 and 2 dB of loss, respectively. The noise figure of the filter directly adds to that of the rest of the system, so the advantages of using a filter with negligible noise figure are clearly highlighted.

1

The values of the insertion losses of HTS and conventional filters in Figure 3 are typical of the application but were chosen
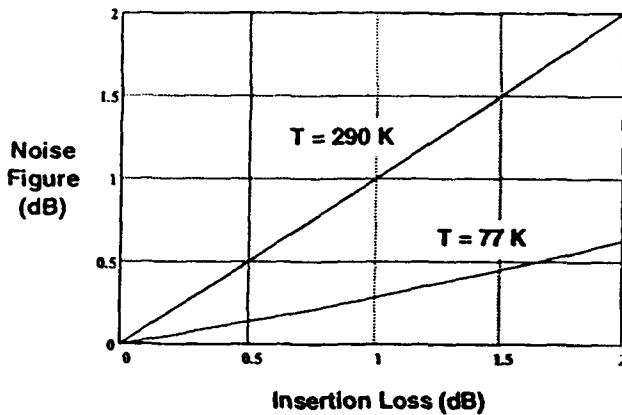

Figure 2 - Calculated filter noise figure as a function of insertion loss for two operating temperatures. Notice that at room temperature the filter noise figure is equal to its insertion loss but that this is not true at 77K.
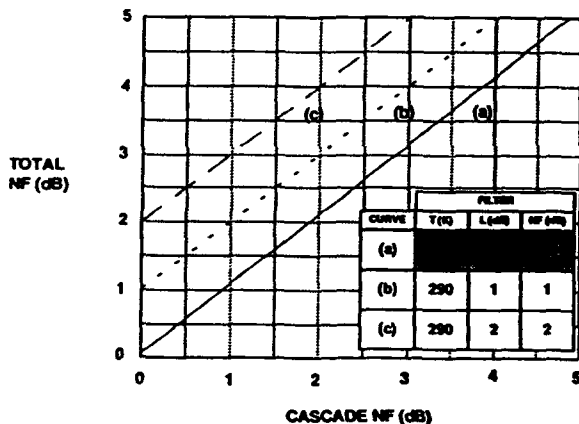

Figure 3 - Calculated effect of filter noise figure on receiver system noise figure. The filter noise figure directly adds to that of the rest of the receiver. The insertion loss values chosen are somewhat arbitrary. They are intended to point out the differences between HTS (small, low loss, cooled) and conventional technologies (relatively small, room temperature) most likely to be used. Filter losses depend on technology used, bandwidth, center frequency and number of poles.

somewhat arbitrarily to make a point. Filter insertion losses depend on filter size and technology (e.g. waveguide vs. microstrip), bandwidth, center frequency and number of poles. Waveguide and dielectric resonator filters can have extremely low loss but are very large in size, especially when multiplexed into switched preselectors. For that reason system designers are often unwilling to use them. HTS technology is expected to provide the capability of low loss filtering with significant size advantages despite the need for cryogenic cooling.

Figure 4 shows the result of a measurement of the noise figure performed on an X-band, HTS filter. This filter was purposely chosen, among a batch of early filters made at Westinghouse [3,4], to

have relatively high insertion loss due to poor quality HTS material. This was done in order to clearly show the difference between the insertion loss and noise figure. Had we performed the measurement with one of the 0.8-dB-loss filters made (noise figure, 0.23 dB), the measurement accuracy (see figure) would not have been adequate to show the difference between insertion loss and noise figure. As shown in Figure 4, the measurement agrees well with the theoretical thermal noise prediction, within the measurement error.
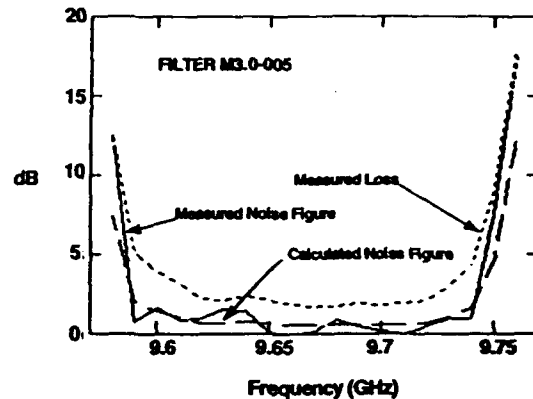

Figure 4 - Measurement of noise figure in a HTS filter. The filter was chosen from a batch of early filters for its high loss (due to poor HTS material quality) in order to clearly show the difference between its insertion loss and the measured and calculated noise figure. Operating temperature was 77K. Filters of the same characteristics (1.5% bandwidth at X-band) have been made by the authors with 0.8 dB of loss.

Third-Order Intermodulation Distortion

HTS filters are non-linear and therefore exhibit intermodulation distortion (IMD). We report on IMD measurements on sample HTS filters and assess, based on the measurements, the impact of front-end preselection on the system spur-free dynamic range (SFDR).

Figure 5 shows the third-order IMD for four HTS filters made in 1990. Three of them were made at Westinghouse, the fourth at Superconductor Technologies. As can be observed from these measurements, performed for input power levels between -15 dBm and 15 dBm, the slope of the third-order products is less than 3:1, for reasons not as yet understood. There is also some variation between filters.

Figure 6 shows the same type of measurement over a wider range of input power levels for a 10-GHz filter also made in 1990. Measurements on a 4 GHz filter, made in 1993, are plotted on the same graph, albeit over a narrow range of power levels. Notice in Figure 6 that the third-order IMD products depart from a 3:1 slope for input power levels below -10 dBm. This has been observed by other workers in the field [1,5]. Ignoring this effect for the time being and assuming a 3:1 slope, the output third-order intercept points (OIP3) are 25 dBm for the 1990 filter, and 37 dBm for the 1993 filter, respectively.

Table I summarizes the contrast in $YBa_2Cu_3O_{7-x}$ growth techniques used at Westinghouse in 1990 and that used currently. One obvious difference in the resulting surface quality is the high density of CuO particles obtained in 1990. Assuming that intermodulation distortion is independent of frequency, the measurements in Figure 6 point out a possible correlation between the HTS film surface quality and the IMD performance. Further work to

confirm this correlation is in progress. The IMD measurements included here are not representative of a complete study of intermodulation distortion in HTS filters. They are merely an initial sample set of measurements, part of a wider ranging project in progress aimed at a better understanding of nonlinear behavior in HTS planar devices.
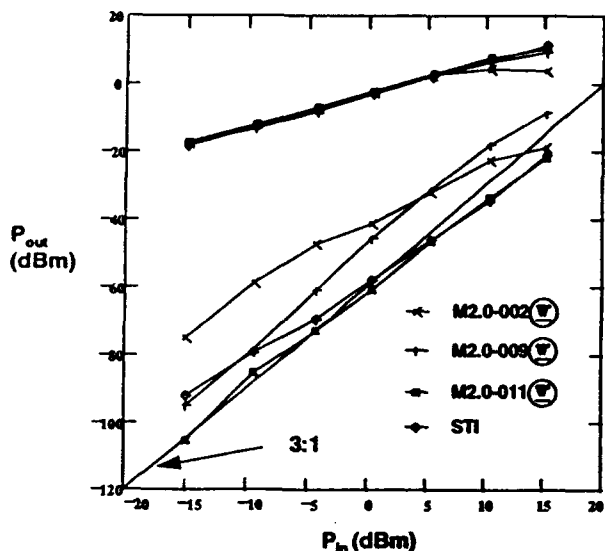
Table I - YBCO Growth Technique Differences

	1990 (10 GHz Filter)	1993 (4 GHz Filter)
Sputtering	DC	RF
Growth Temp.	650 C	700 - 750 C
Substrate Heating	Silver-Painted	Radiation
Substrate Size	Small Chips	2-inch Dia
Surface Quality	High Density of CuO Particles	Smooth

Figure 5 - Third-order intermodulation distortion for four filters made in 1990.
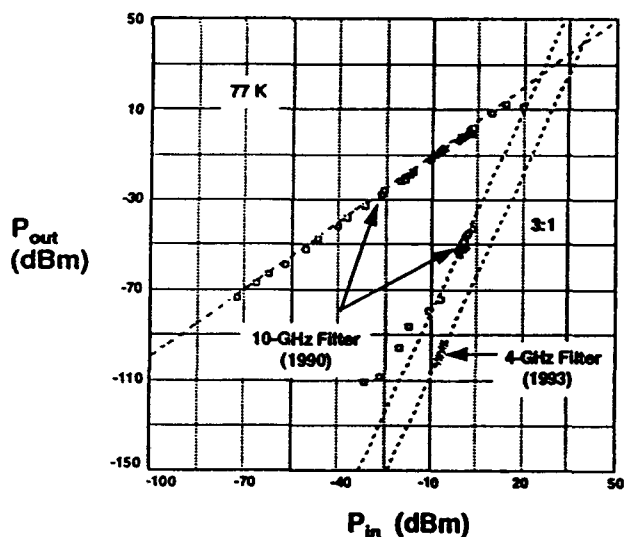
Figure 6 - Third-order intermodulation distortion for a filter made in 1990 and a filter made in 1993, showing the difference in performance due to the improved HTS material quality.
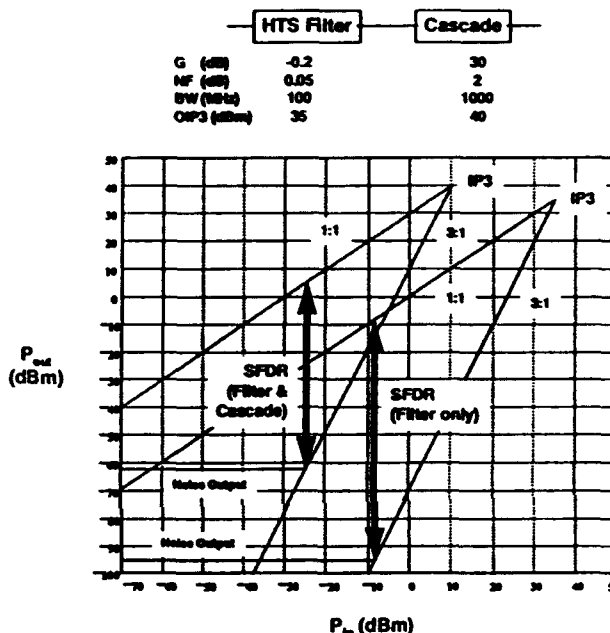

Figure 7 - Graphic depiction of the spur-free dynamic range (SFDR) for a filter alone and for the filter followed by the rest of a microwave receiver.

Figure 7 shows graphically the effect on the SFDR of an input HTS filter followed by a Cascade of components. The various parameters assumed are shown in the figure. From this calculation we conclude that, for the parameters chosen, the third-order IMD spurs generated in the filter, including those that have a slope lower than 3:1 (see Figure 6), will not have a significant effect on the system's SFDR. Notice that the noise figure of 2 dB and the IP3 point of 40 dBm chosen for the Cascade in this calculation correspond to good quality components so as to highlight the relatively wide margin of tolerance on the filter's IMD characteristics. Figure 8 is a plot of the SFDR as a function of the Cascade OIP3, with the filter OIP3 as a parameter. The other parameters, given in the insert, are the same as for Figure 7. These curves show that the IMD performance of the filter has indeed a small effect on the SFDR for achievable values of the filter OIP3.

3

Conclusion

In conclusion, our analyses and measurements show that using HTS filters in the front end of microwave receivers will allow all the advantages of preselection without appreciable added system noise. And even though HTS filters are non-linear, the third-order intermodulation distortion introduced is not likely to affect the system spur-free dynamic range, as it will probably be set by the rest of the receiver chain.

Acknowledgment

References

1. D. E. Oates, W. G. Lyons and A. C. Anderson, "Superconducting Thin-Film $YBa_2Cu_3O_{7-x}$ Resonators and Filters," 45th Annual Symp. on Freq. Control Digest, pp. 460-466, 1991.

2. W. W. Mumford and E. H. Scheibe, "Noise Performance Factors in Communication Systems," Horizon House-Microwave, 1968.

3. S. H. Talisa et al. "Low- and High-Temperature Superconducting Microwave Filters," IEEE Trans. on Microwave Theory and Tech., Vol. 39(9), pp. 1448-1454, Sep. 1991.

4. S. H. Talisa, M. A. Janocko, J. Talvacchio and C. Moskowitz, "Present and Projected Performance of High-Temperature Superconducting Filters," 1991 IEEE Int. Microwave Symp. Digest, pp. 1325-1328.

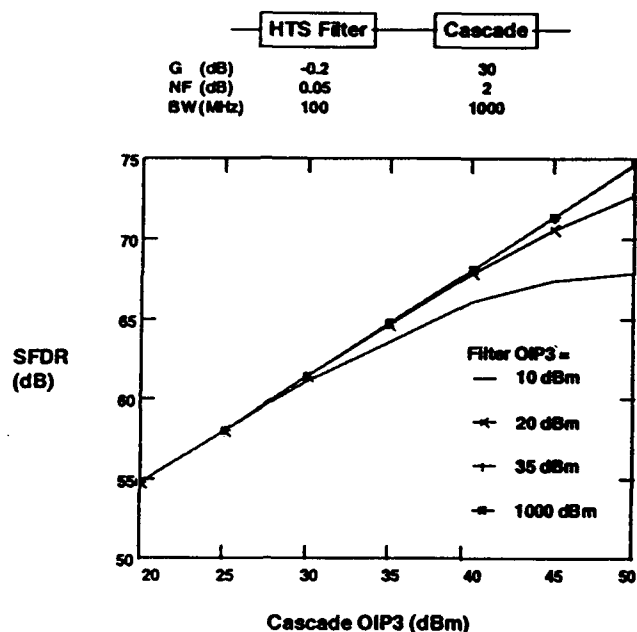5. G. Hey-Shipton, Superconductor Technologies, private communication.

Figure 8 - Calculated effect of the preselector filter output third-order intercept point (OIP3) on the receiver spur-free dynamic range (SFDR) as a function of the Cascade OIP3.